One-transistor-cell 4-valued universal-literal CAM for cellular logic image processing

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One-Transistor-Cell 4-Valued Universal-Literal CAM for Cellular Logic Image Processing

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Abstract

A non-volatile 4-valued content-addressable memory (CAM) is proposed for fully parallel template-matching operations in real-time cellular logic image processing with fixed templates. A universal literal in each CAM cell is used to compare a 4-valued input pixel with a 4-valued template pattern. Any CAM cell functions are performed by a pair of a simple threshold operation and a logic-value conversion which is shared by CAM cells in the same column of a CAM cellular array. Moreover, the use of a single floating-gate MOS transistor makes it possible to implement a universal-literal circuit together with a 4-valued storage element. As a result, a high-density 4-valued universal-literal CAM with a single transistor cell is designed by using a multi-layer interconnection technology. Its performance is much superior to that of conventional CAM-based implementations under the same dynamic power dissipation.

1. Introduction

In intelligent robot systems and real-time instrumentation and control systems, it is important to perform real-time cellular logic image processing which requires highly parallel template-matching operations with many templates [1],[2]. Some hardware accelerators have been already developed for highly parallel cellular logic image processing[3]. However, various operations for cellular logic image processing make their circuits complicated, which causes a limited application with a smaller size of an image.

On the other hand, it has been well-known that CAMs are suitable as a hardware accelerator for highly parallel processing with single instruction multiple data streams[4]. From this point of view, multiple-valued (MV) universal-literal CAMs have been proposed for highly parallel template-matching operations [5],[6]. These MVCAMs are useful as a hardware accelerator in high-speed non-numeric processing systems such as a cellular logic image processing system with many templates because of their compact implementation based on multiple-valued logic. However, towards the next-generation real-world applications such as vision systems, it is important to develop a much higher-density universal-literal MVCAM.

This paper presents a new non-volatile 4-valued CAM with a single-transistor CAM cell for fully parallel cellular logic image processing. Since gray-level or colored pixel values are directly represented by MV data in cellular logic image processing, a template-matching operation with an $N \times N$ window is performed by multiple-valued logic operations, that is 'universal literals'[7],[8].

A universal literal is described by combination of 2 window literals, so that it requires 4 threshold operations which make a universal-literal circuit complicated. In this paper, a universal literal is represented by a down literal with permutation of a 4-valued input signal, called a 'logic-value conversion' (LVC). Since a down literal is performed by a threshold operation with a single threshold, the proposed CAM cell function becomes simple.

Moreover, a threshold-operation circuit is easily designed by only a floating-gate MOS transistor whose threshold voltage is programmable by controlling the charge on the floating gate[9]. Consequently, the successive universal-literal CAM cell circuit can be designed by only a single floating-gate MOS transistor whose threshold voltage level corresponds to a stored value of a 4-valued template.

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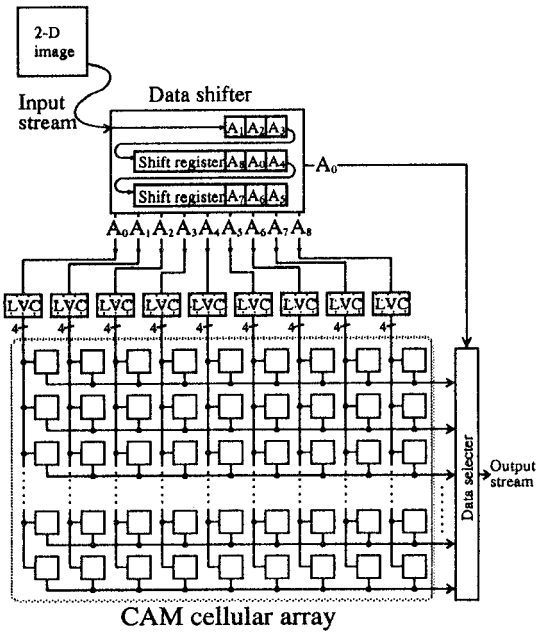


Figure 1. Structure of a CAM-based image processor.

In fact, the access time and the cell area of the proposed 4-valued 1Mb universal-literal CAM are about $47(\mu m^2)$ and 11.8(nsec)/word, , respectively, with the power dissipation of 4.7(mW) at the supply voltage of 5(V). These performances are much superior to that of other CAM-based implementations.

2. Basic 4-valued universal-literal CAM organization

In this section, we discuss about an overview of a high-speed cellular logic image processor with fully parallel template-matching capability.

2.1. Overall universal-literal CAM structure

In the cellular logic image processing, a digital image is uniformly sampled and quantized to several levels. Let the set of discrete quantities in 4-valued images be $L = \{0, 1, 2, 3\}$. As shown in Figure 1, the proposed cellular logic image processing system is performed in a pipelining manner where a universal-literal 4-valued CAM is used as a hardware accelerator for parallel template-matching operations. 2-dimensional

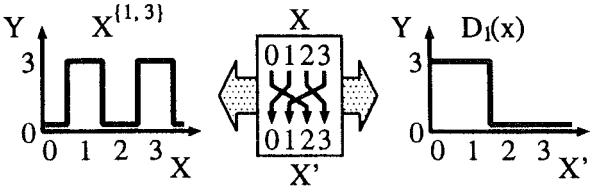


Figure 2. Realization of a universal literal.

input image data are transformed into serial data according to line scanning. 9 pixels corresponding to a 3×3 window are picked up from the line-scanned image data simultaneously, and are entered into the CAM cellular array for parallel template-matching operations.

A simple near-neighbor operation in the cellular logic image processing is generalized by a template-matching operation between a window of an input image and templates with the same window size. Since enormous templates are required in some image processing, several templates are compressed by using a simplification technique of MV logic functions[10]. Using these compressed templates, the number of template-matching operations can be greatly reduced. Universal literals are used to perform template-matching operations with MV compressed templates.

In the following discussion, we describe the formulation of 4-valued template-matching operations based on universal literals.

2.2. 4-valued universal literal for MV pattern matching

A universal literal is one of the basic components for MV pattern-matching operations with compressed templates and is defined as

$$X^{\{a\}} = \begin{cases} 3 & \text{if } X \subset a \\ 0 & \text{otherwise} \end{cases} \quad (1)$$

where $a \subset L$.

A universal literal can be expressed by combination of 2 window functions. For example, Figure 2 shows a 4-valued universal literal $X^{\{1,3\}}$. If an input stream $X = (0, 1, 2, 3)$ of $X^{\{1,3\}}$ is permuted by $(1, 3, 0, 2)$, the resulting logic function can be represented by a simple threshold function $D_1(X)$ where a threshold function $D_a(X)$ is defined as

$$D_a(X) = \begin{cases} 3 & \text{if } X \leq a \\ 0 & \text{otherwise} \end{cases} \quad (2)$$

where $a \in L$. The permutation of an input stream is called 'logic-value conversion'(LVC).

Table 1. Synthesis of 16 logic functions for a universal literal.

Functions	LVC	Threshold function	Functions	LVC	Threshold function
$X^{\{\phi\}}$	—	—	$X^{\{0,2\}}$	$f_5 < 2,0,3,1 >$	$D_1(x)$
$X^{\{0\}}$	$f_2 < 0,3,2,1 >$	$D_0(x)$	$X^{\{0,3\}}$	$f_2 < 0,3,2,1 >$	$D_1(x)$
$X^{\{1\}}$	$f_3 < 1,0,3,2 >$	$D_0(x)$	$X^{\{1,3\}}$	$f_6 < 1,3,0,2 >$	$D_1(x)$
$X^{\{2\}}$	$f_4 < 2,1,0,3 >$	$D_0(x)$	$X^{\{0,1,2\}}$	$f_4 < 2,1,0,3 >$	$D_2(x)$
$X^{\{3\}}$	$f_1 < 3,2,1,0 >$	$D_0(x)$	$X^{\{0,1,3\}}$	$f_3 < 1,0,3,2 >$	$D_2(x)$
$X^{\{0,1\}}$	$f_3 < 1,0,3,2 >$	$D_1(x)$	$X^{\{0,2,3\}}$	$f_2 < 0,3,2,1 >$	$D_2(x)$
$X^{\{1,2\}}$	$f_4 < 2,1,0,3 >$	$D_1(x)$	$X^{\{1,2,3\}}$	$f_1 < 3,2,1,0 >$	$D_2(x)$
$X^{\{2,3\}}$	$f_1 < 3,2,1,0 >$	$D_1(x)$	$X^{\{L\}}$	$f_1 < 3,2,1,0 >$	$D_3(x)$

Let $(0,1,2,3)$ be an input string of a 4-valued LVC f. Let (p_0,p_1,p_2,p_3) be an output string of f corresponding to the input string. The LVC f is defined as

$$f =< p_0,p_1,p_2,p_3 > \quad (3)$$

where $p_i(0 \leq i \leq 3) \in L$. To realize a 4-valued universal literal, we must prepare 6 LVCs, f_1, f_2, f_3, f_4, f_5 and f_6 which are defined as

$$\begin{aligned} f_1 &= < 3,2,1,0 >, \\ f_2 &= < 0,3,2,1 >, \\ f_3 &= < 1,0,3,2 >, \\ f_4 &= < 2,1,0,3 >, \\ f_5 &= < 2,0,3,1 >, \\ \text{and } f_6 &= < 1,3,0,2 > . \end{aligned} \quad (4)$$

Table 1 shows 16 pairs of an LVC and a threshold function which correspond to 16 kinds of functions generated by a 4-valued universal literal. As shown in this figure, it is clear that a 4-valued universal literal is realized by a pair of an LVC and a threshold function.

3. Universal-Literal CAM with One-Transistor-Cell Structure

In this section, we discuss about a design of a simple MVCAM cell circuit using a floating-gate MOS transistor, and an overall structure based on the proposed MVCAM cellular array.

3.1. One-transistor CAM cell circuit

According to Section 2, a universal literal can be represented by combination of a single threshold operation and a kind of LVC. Figure 3 shows a circuit design and a layout of a 4-valued universal-literal CAM

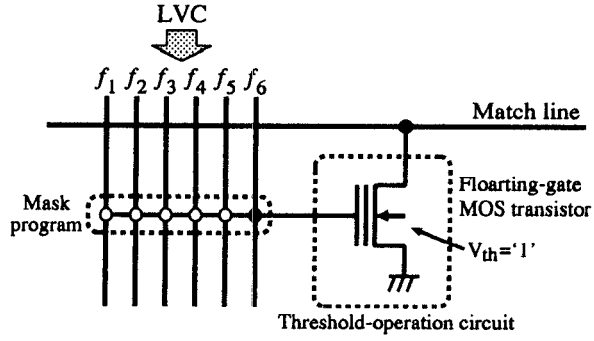


Figure 3. CAM cell circuit.

cell circuit with only a single floating-gate MOS transistor. 1 of 6-LVC output signals generated from an input signal is selected by mask programming in each CAM cell. A universal literal can be realized by a threshold operation with a selected LVC output signal in each CAM cell. Since the threshold voltage of a floating-gate MOS transistor can be programmed by controlling the charge on its floating gate, a threshold operation with a one-digit 4-valued storage element can be performed simultaneously by using a single floating-gate MOS transistor.

Tables 2 and 3 show the relationship among 4-valued input logical values, 4-valued threshold values and their corresponding voltage levels. Since 6 LVCs are shared by every CAM cell in the same column of a CAM cellular array, each CAM cell function is enough to perform only a single threshold operation with mask programming of LVCs. As a result, the successive CAM cell can be designed by only a single floating-gate MOS transistor.

For example, Figure 3 shows a design of a universal literal $X^{\{1,3\}}$ which is constructed by the LVC f_2 and

Table 2. Relationship between logical values and voltage levels.

Input logical values	0	1	2	3
Voltage levels(V)	0.0	1.0	2.0	3.0

Table 3. Relationship between logical values and voltage levels.

Threshold values	0	1	2	3
Voltage levels(V)	0.5	1.5	2.5	3.5

the threshold function $D_1(X)$ as shown in Figure 2.

3.2. One-word CAM structure

The use of the wired AND technique makes it possible to generate the product of 9 universal literals corresponding to a 3×3 template without additional transistors. Figure 4 shows a design of a one-word CAM circuit based on 9 floating-gate MOS transistors. First, the match line of the one-word CAM circuit is previously precharged to a high level (V_{DD}) by using the NMOS pass transistor M_1. If an input pixel pattern is matched to the template pattern, all the 9 floating-gate MOS transistors are turned off. As a result, the match line still remains a high level. Otherwise, a floating-gate MOS transistor is at least turned on, resulting in pulling down the match line to a low level.

Consequently, the voltage level V_{ML} of the match line represents the relationship between an 9-pixel input vector $\mathbf{X} = (x_1, x_2, \cdots x_9)$ and a template-pattern vector $\mathbf{P} = (p_1, p_2, \cdots p_9)$, which is written as

$$\begin{cases} \mathbf{X} = \mathbf{P} & \text{if } V_{ML} \text{ is high} \\ \mathbf{X} \neq \mathbf{P} & \text{if } V_{ML} \text{ is low.} \end{cases} \quad (5)$$

3.3. LVC circuit

Figure 5 shows a circuit diagram to produce 6-LVC output signals. The NMOS transistors $M_1 - M_8$ in a decoder are used as the components of binary inverters and NOR circuits with different threshold voltages realized by multiple ion implants where the threshold voltages of M_1, M_3, M_4, M_6 and M_7 are $0.0V, 1.8V, 1.8V, 3.5V$ and $3.5V$, respectively and where the other transistors have the same threshold voltage $1.0V$ as the conventional enhancement-mode one. The

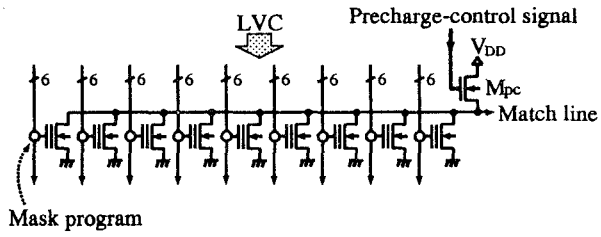


Figure 4. One-word CAM circuit.

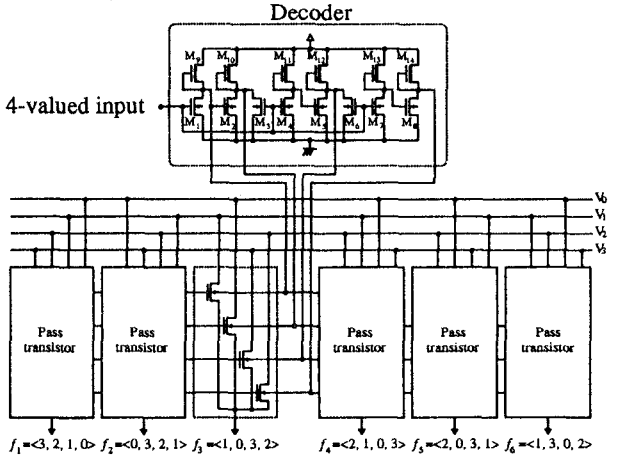


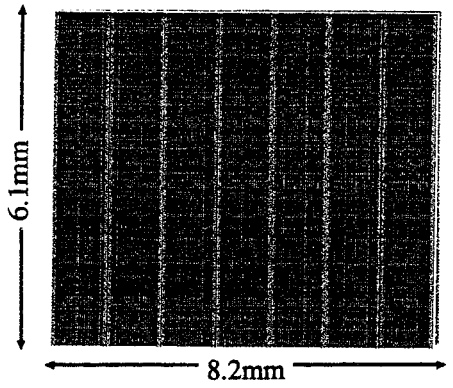
Figure 5. Logic-value conversion circuit.

transistors $M_9 - M_{14}$ are the depletion-mode NMOS ones.

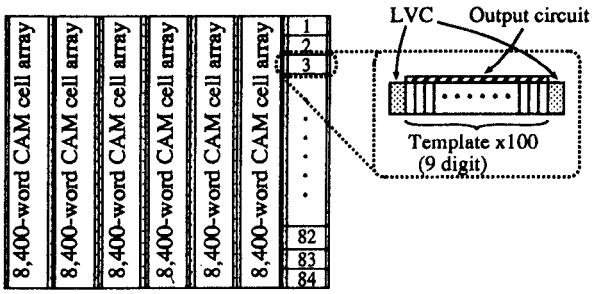
A pair of 4-rail one-hot binary signals corresponding to a 4-valued input signal is generated from the decoder. Using the control signals, gate voltages of pass transistors whose inputs are directly connected to one of four different supply voltages. 6 kinds of LVCs are realized by programming the input signals to pass transistors.

3.4. 1-Mb 4-valued universal-literal CAM design

Figure 6 shows a layout and its floor plan of the proposed 1Mb 4-valued universal-literal CAM. The performance of the proposed CAM is summarized in Table 3. Since an LVC circuit is shared by 100 cells in the same column of MVCAM cellular array, the effective chip area of LVC circuits is limited to occupy about 30% of a total chip area.



(a)Layout.



(b)Floor plan.

Figure 6. 1M-bit CAM.

4. Evaluation

To evaluate the performance of the proposed MV-CAM, we discuss about different approaches based on a binary CAM and previously proposed MVCAMs, respectively.

4.1. Universal-literal circuit using conventional binary CAM cells

Highly parallel template-matching operations for cellular logic image processing can be also performed by the hardware based on other CAM structures. Figure 7 shows design of a 4-valued universal-literal CAM cell using binary dynamic CAM cells. Since 1 of 4 levels is programmed by a single binary CAM cell, the number of CAM cells to perform a 4-valued universal literal becomes 4. Moreover, a binary dynamic CAM cell is designed by 5 transistors and 2 capacitors [11].

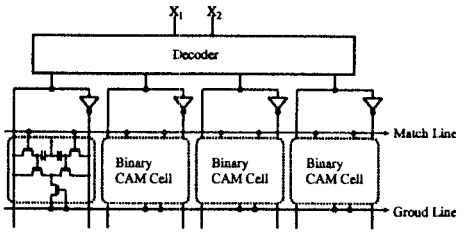


Figure 7. 4-valued universal-literal circuit using binary CAM cells.

4.2. Comparison of performances

Table 4 summarizes the comparison of the template-matching circuits using CAM-based architectures with a 4-valued 3×3 template under a 0.8-μm standard EEPROM technology. Although a window size is a 3×3 in this evaluation, it can be easily extended to any sizes.

Due to the poor functionality of binary CAM cells, binary-CAM based hardware requires more than 8-times larger chip area than that of the proposed 4-valued universal-literal CAM. In proportion to the number of cell transistors, the cell areas of conventional universal-literal CAMs are larger than that of the proposed hardware.

The access time and the power dissipation of CAMs depend on total capacitance of the match line. Since the proposed CAM cell is designed by less transistors in comparison with those of other CAMs, the length of the match line becomes the shortest and the line capacitance becomes the lowest of all the other implementation. In fact, the access speed of the proposed CAM is about twice, 1.8 and 1.3 times faster than that of a binary CAM, 4-transistor-cell and 2-transistor-cell MV-CAMs, respectively under PSPICE simulation. Moreover, the power dissipation of the proposed hardware is evaluated to be reduced to about 56 percent, 59 percent and 79 percent compared with that of a binary implementation, 2 conventional 4-valued implementations, respectively.

From the viewpoint of the above performance evaluation, it is clear that the proposed one-transistor-cell 4-valued CAM has the best performance of all the other CAMs for highly parallel cellular logic image processing.

Table 4. Comparison of performances (1Mbit)

	Binary CAM-based implementation	Conventional 4-valued CAM (4-Tr. Cell) (Ref.[5])	Conventional 4-valued CAM (2-Tr. Cell) (Ref.[6])	Proposed CAM (1-Tr. Cell)
Layout area	$377\mu m^2$	$125\mu m^2$	$107\mu m^2$	$47\mu m^2$
Power dissipation (1word)	8.4mW	8.0mW	6.0mW	4.7mW
Access time	23.6ns	21ns	15.7ns	11.8ns

5. Conclusion

In this paper, a new 4-valued universal-literal CAM with a single transistor cell has been proposed for fully parallel template-matching operations in cellular logic image processing. A universal literal in each CAM cell is performed by the decomposition of an LVC and a threshold function, which makes a CAM cell function simple. Moreover, the use of floating-gate MOS transistor results in a one-transistor CAM cell design whose performance is evaluated to be the highest of all the other CAM-based implementations.

As a future problem, it is also important to reduce the dynamic power dissipation of the proposed universal-literal CAM. The main dynamic power of the CAM is consumed by discharging the output capacitive load of the match line when the corresponding word is a 'mismatch' state, while no dynamic power is consumed by the match line when the corresponding word is a 'match' state. Since almost all the template-matching results are 'mismatch' in the CAM, the most output capacitive loads of the match line must be discharged. If a NAND-type structure is used for a one-word CAM circuit instead of a NOR-type structure in the proposed CAM, only the output capacitive load of the match line is discharged in the match-state word. As a result, it is expected that the use of the circuit technique makes the power dissipation reduced greatly.

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